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(71) Applicant (for all designated States except US): **TELEFONAKTIEBOLAGET LM ERICSSON** [SE/SE];
S-126 25 Stokholm (SE).

(72) Inventors; and

(75) Inventors/Applicants (for US only): **WEGO, Arild** [NO/NO]; Måkeveien 4, N-3400 Lier (NO). **HELLUM, Pål, Longva** [NO/NO]; Engertunet 3, N-1365 Blommenholm (NO).

(74) Agent: **OSLO PATENTKONTOR AS**; Postboks 7007 M, N-0306 Oslo, NO (NO).

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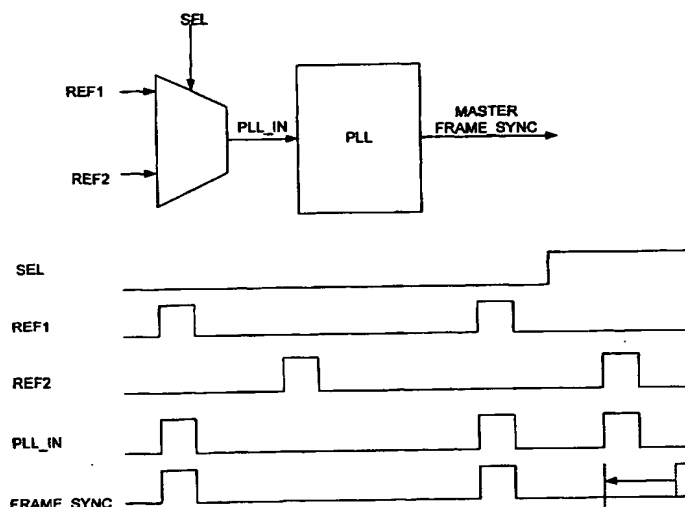
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(54) Title: METHOD AND ARRANGEMENT FOR REDUCING PHASE JUMPS WHEN SWITCHING BETWEEN SYNCHRONISATION SOURCES



(57) Abstract: A method and an arrangement for reducing phase jumps in a frame synchronisation signal when switching between synchronisation reference sources are disclosed. A new reference signal to which each of the two reference sources (signals) are phase locked, and has frequency n times the respective reference signal, is generated. A selection signal selects the new reference signal to be used, and the selected one is then divided back to its original frequency creating an input signal to a phase-locked loop generating the resulting frame synchronisation signal. In this way, the maximum phase jumps are reduced from one period of the original reference signals to one period of the new reference signal. The invention is particularly applicable for reducing phase jumps on a master frame synchronisation signal in a PDH system.



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METHOD AND ARRANGEMENT FOR REDUCING PHASE JUMPS WHEN SWITCHING BETWEEN SYNCHRONISATION SOURCES

Field of the invention

The present invention is related to synchronisation in communication networks, in particular to reduction of phase jumps in a frame synchronisation signal when switching
5 between synchronisation reference sources.

Background of the invention

The lower layer of communication networks like the connectivity layer in a core network of a cellular environment could be seen as a layer of distributed
10 resources for managing data flows. Some of the main nodes comprised in such networks are switches routing and directing data from input to output lines. Reliable internal synchronisation in these switches is crucial i.a. for keeping bit slips through the switches as low as
15 possible.

The switches are normally equipped with internal Time Division Multiplex buses leading frames consisting of time slots of data from the receiving to the transmitting side of the switch in a predefined way. For a regular
20 transmission of the frames, they are synchronised with a master timer initiating transmission of each frame.

The H.110 standard specifies that inside a node, e.g. a switch, there will be two potential providers of the master timing, primary master and secondary master. The purpose of
25 having two master timers is that if the primary master fails, the secondary master will take over the timing in the node. Reasons for this may be line failure in some of the input lines, signal of poor quality, power outage, etc.

The clock sources for the primary and secondary master are
30 reference signals, netref#1, and netref#2. Any of the serial input ports in a node can be the source for netref#1

and netref#2. These clocks are synchronised to the specific timing in the network.

However, the problem area is not specially related to the H.110 solution, but acts as an example. To illustrate the problem this document issues, an additional example system is taken into consideration, namely the Plesichronous Digital Hierarchy (PDH). PDH is a transmission protocol normally applied for data transmission at data rate magnitudes of 64kbit/s to 139,264Mbit/s.

Figure 1 shows a simplified block diagram and timing diagram of the synchronisation mechanism in a PDH system. One of two (or more) references that are usually extracted from serial data links is used as the timing reference for a master frame synchronisation signal. The references (REF1 and REF2) and the frame synchronisation signal (FRAME_SYNC) are usually 8kHz signals (125us period) indicating one TDM frame.

REF1 and REF2 may have an arbitrary phase relation. A PLL is mainly used for jitter attenuation and to smooth out phase variations at switch-over from one reference to another. An external select signal (SEL) selects whether REF1 or REF2 shall be chosen as timing reference. At switch-over from one reference to another (i.e. when the chosen reference disappears or if the quality of the reference is poor), the phase difference between the references will lead to a phase jump on the input of the PLL. This will gradually lead to a phase change on the frame synchronisation signal. The phase change may be up to one period of the reference signals (worst case). The two worst-case phase jump conditions are illustrated in Figure 2 and figure 3.

A FIFO is normally placed ahead of the TDM bus for reducing the effect of data rate variations and small phase irregularities. However, such FIFOs are not dimensioned to

absorb large phase jumps, as the use of deep FIFOs lead to longer timing delays and more logic. Thus, the phase jump in the frame synchronisation signal as described above, may result in an overflow in the FIFO, which in turn would lead to bit slips and bit errors, and resynchronisation and retransmission of data at switch-over from one timing reference to another may be necessary.

WO 98/25367 and WO 98/25368 disclose variants of a method of generating a system clock signal periodically locked to a selected one of a plurality of phase-locked loops, each of which emitting a clock signal in phase-locked relationship with an external reference signal. A digital error signal is transferred from the selected phase-locked loop to a central numerically controlled oscillator, and the system clock is locked to the output signal from the central numerically controlled oscillator.

US 5,909,149 discloses a multi-band locked loop employing multiple switchable voltage controlled oscillators. A single PLL is provided having a different voltage controlled oscillator for each desired frequency band. The transfer function of the phase detector in the phase-locked loop is switched responsive to the particular band selected for maintaining the loop natural frequency at the same point regardless of other changes in the loop transfer function, such as changes in the frequency slope of the voltage controlled oscillators and changes in the division ratio of the loop divider circuit.

One of the drawbacks of WO 98/25367 and WO 98/25368 is that much logic is necessary since several phase detectors and numerically controlled oscillators are required. This contributes to a very complicated solution. In addition, a digital error signal must be integrated over a period of time.

US 5,909,149 is truly related to problems with switching between two frequency references, but it only concerns switching problems that occur when switching from one frequency band to another, and not phase jumps between two references with the same frequency. Thus, the publication
5 does not solve this problem since it is not attenuating phase jumps when switching between the frequency references.

Summary of the invention

10 It is an object of the present invention to provide a method and an arrangement that eliminates the drawbacks described above. The features defined in the claims enclosed characterize this method and arrangement. In particular, the invention discloses a method and an
15 arrangement in a telecommunication or data communication network for reducing phase jumps in a frame synchronisation signal when switching from a first original reference signal to a second reference signal. The method comprises the steps of generating a first and a second master
20 reference signal phase locked to the first and the second original reference signal, respectively, each with a frequency n times the frequency of the corresponding original reference signal, selecting one of the master reference signals by a selection signal, dividing the
25 frequency of the selected master reference signal back to the frequency of its corresponding reference signal, inputting the frequency divided signal into a Phase-Locked Loop circuit for generating the frame synchronisation signal. The arrangement implements this method.

Brief description of the drawings

In order to make the invention more readily understandable, the discussion that follows will refer to the accompanying drawings.

5 Fig. 1 shows a block and timing diagram illustrating the basic concept of the synchronisation mechanism in a PDH system,

Fig. 2 shows timing diagrams illustrating one of the worst-case phase jumps in frame synchronisation signal in the
10 system of fig. 1,

Fig. 3 shows timing diagrams illustrating the other worst-case phase jump in frame synchronisation signal in the system of fig. 1,

Fig. 4 shows a block and timing diagram illustrating an
15 example of the synchronisation mechanism in a PDH system improved according to the present invention.

Detailed description

The present invention describes a method of reducing phase jumps in a frame synchronisation signal when switching
20 between synchronisation reference sources.

The present invention is based on the realization of the fact that when generating a master frame synchronisation signal, it is necessary to lock to the frequency of the reference, but the phase relation to the reference has no
25 importance.

To reduce the phase jump at switch-over from one reference to another, the present invention introduces "clocks" (MREF1 and MREF2) that are phase locked to the reference signals with a frequency that is n times the reference

signals (n is an integer number). These clocks may be generated by counters clocked by a high frequency clock (CLK), and reset by the reference signal, as shown in figure 4.

5 After the mux, the selected "clock" (MREF) is divided back to the original frequency again. In this way the maximum phase jumps are reduced from one period of the reference signal to one period of the MREF signal, as illustrated in figure 4. The frequency of the MREF "clocks" should be as
10 high as possible to minimize the phase jumps at switch-over, but it must not be so high that a variable number of MREF "clock" periods between two REF pulses appears. This will occur when the frequency of MREF is so high that the period of MREF is smaller than the delta period of the
15 maximum tolerable frequency deviation of the REF signal ($\text{REF}(\text{nominal period}) - \text{REF}(\text{min period})$ or $\text{REF}(\text{max period}) - \text{REF}(\text{nominal period})$). Consequently, the MREF period must always be longer than this maximum period variation.

20 An example embodiment of the present invention, together with timing diagrams illustrating a scenario where the reference signal is shifted, is shown in figure 4. This scenario illustrates the effect of the present invention.

The two reference signals available, REF1 and REF2, generate MREF1 and MREF2 by phase-locking clock signals
25 having a frequency of n times the frequency of the respective reference signals with the reference signals themselves. MULT n indicates that the MREF1 and MREF2 frequencies are, respectively, the REF1 and REF2 frequencies multiplied with n where n is a power of two
30 integers (2, 4, 8, 16 etc.). MREF1 and MREF2 are multiplexed with the selection signal (SEL), so that MREF1 is selected when SEL is low, and MREF 2 when SEL is high. The selected MREF signal is then divided by n (preferably by a counter) leading to PLL_IN, which is the input of the
35 PLL circuit finally outputting the resulting master frame

synchronisation signal. DIV n indicates that the PLL_IN frequency is the MREF frequency divided by n where n is the same integer as in MULT n.

5 In the case illustrated in figure 4, PLL_IN goes high right after REF1. This is just for showing that the phase of PLL_IN does not change even if SEL changes from REF1 to REF2. The PLL_IN goes high because the DIV element has counted n periods. MREF is reset at next REF2, but because the periods of MREF1 and MREF2 are shorter than the maximum
10 phase variation between two REF pulses, a variable number of MREF "clock" periods between two REF pulses will not occur. It should be noted that it is no longer any correlation between the phase of REF1/REF2 and PLL_IN. The original PLL has now become a frequency-locked loop (FLL)
15 that suppresses phase jumps bigger than one MREF period.

MULT n indicates that the MREF1 and MREF2 frequencies are, respectively, the REF1 and REF2 frequencies multiplied with n where n is a power of two integers (2, 4, 8, 16 etc.). DIV n indicates that the PLL_IN frequency is the MREF
20 frequency divided by n where n is the same integer as in MULT n.

It should be noted that the logical levels and the specific logical devices chosen in the timing and block diagram of figure 4 could be chosen differently. The purpose of the
25 timing and block diagram is to illustrate an embodiment and a scenario of events that may occur when utilising the present invention, and is not limiting the scope of it as defined in the independent claims enclosed.

The main advantage of the present invention is that max
30 phase jumps at switch from one reference to another can be reduced from one period of the reference signal to the delta period of the maximum tolerable frequency deviation of the REF signal (REF(nominal period) - REF(min period) or REF(max period)-REF(nominal period).

Further, bit faults can be avoided at switch-over from one reference to another without implementing large FIFOs, giving reduced bit error rate. Avoiding large FIFOs also reduce timing delays and the amount of logic.

- 5 The present invention provides a non-complicated solution, and less resynchronisation and retransmission of data will be needed.

Abbreviations

FIFO First In First Out buffer

FLL Frequency Locked Loop

PDH Plesichronous Digital Hierarchy

5 PLL Phase-Locked Loop

PDH Plesichronous Digital Hierarchy

References

10 [1] WO 98/25367 and WO 98/25368; A method and a circuit
for generating a system/central clock signal

[2] US patent 5,909,149; Multiband phase-locked loop using
a switched voltage controlled oscillator

P a t e n t c l a i m s

1. A method in a telecommunication or data communication network of reducing phase jumps in a frame synchronisation signal when switching from a first original reference
5 signal to a second reference signal,
c h a r a c t e r i z e d i n

generating a first and a second master reference
signal phase locked to the first and the second
original reference signal, respectively, each with a
10 frequency n times the frequency of the corresponding
original reference signal,

selecting one of the master reference signals by a
selection signal,

dividing the frequency of the selected master
reference signal back to the frequency of its
15 corresponding reference signal,

inputting the frequency divided signal into a Phase-
Locked Loop circuit for generating the frame
synchronisation signal.

- 20 2. Method according to claim 1,
c h a r a c t e r i z e d i n that in the selection step
the first master reference signal is selected when the
selection signal is low, and the second master signal is
selected when the selection signal is high, or vice versa.

25 3. Method according to claim 1 or 2,
c h a r a c t e r i z e d i n that the dividing step is
carried out by counting the number of periods of the
selected master reference signal and outputting a pulse
like in the corresponding original reference signal for
30 each nth period of the selected master reference signal.

4. Method according to one of the preceding claims,
c h a r a c t e r i z e d i n that the periods of the
master reference signal are longer than the delta period of
maximum tolerable frequency deviation of the corresponding
5 original reference signal.

5. Method according to one of the preceding claims,
c h a r a c t e r i z e d i n that the frame
synchronisation signal is a master frame synchronisation
signal in a PDH system.

10 6. An arrangement in a node of a telecommunication or
data communication network of reducing phase jumps in a
frame synchronisation signal when switching from a first
original reference signal to a second reference signal,
c h a r a c t e r i z e d i n

15 an element for each original reference signal
generating a first and a second master reference
signal phase locked to the first and the second
original reference signal, respectively, each with a
frequency n times the frequency of the corresponding
20 original reference signal,

a multiplexer with the first and the second master
reference signal as input in addition to a selection
signal selecting one of the master reference signals
as the output of the multiplexer,

25 a divider dividing the frequency of the output of the
multiplexer back to the frequency of the corresponding
reference signal,

a Phase-Locked Loop circuit for generating the frame
synchronisation signal having the divider output
30 signal as input.

7. Arrangement according to claim 6,
c h a r a c t e r i z e d i n that the multiplexer
selects the first master reference signal when the
selection signal is low, and the second master signal when
5 the selection signal is high, or vice versa.
8. Arrangement according to claim 6 or 7,
c h a r a c t e r i z e d i n that the divider is a
counter counting the number of periods of the output signal
of the multiplexer outputting a pulse like in the
10 corresponding original reference signal for each nth period
of the output signal of the multiplexer.
9. Arrangement according to one of the claims 6-8,
c h a r a c t e r i z e d i n that the periods of the
master reference signals are longer than the delta period
15 of maximum tolerable frequency deviation of the
corresponding original reference signal.
10. Arrangement according to one of the claims 6-9,
c h a r a c t e r i z e d i n that the node is a
switch.
- 20 11. Arrangement according to one of the claims 6-10,
c h a r a c t e r i z e d i n that the frame
synchronisation signal is a master frame synchronisation
signal in a PDH system.

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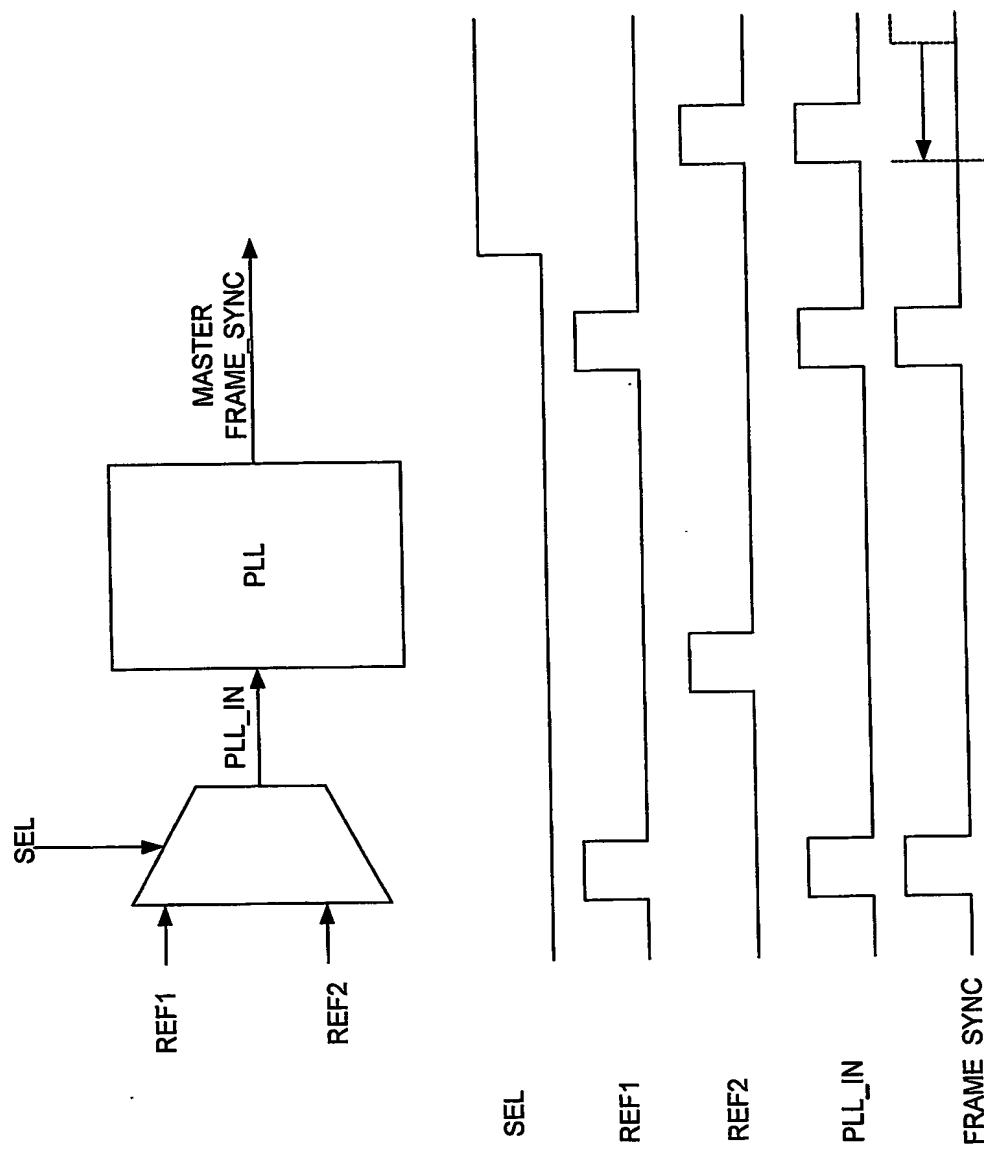


Fig. 1

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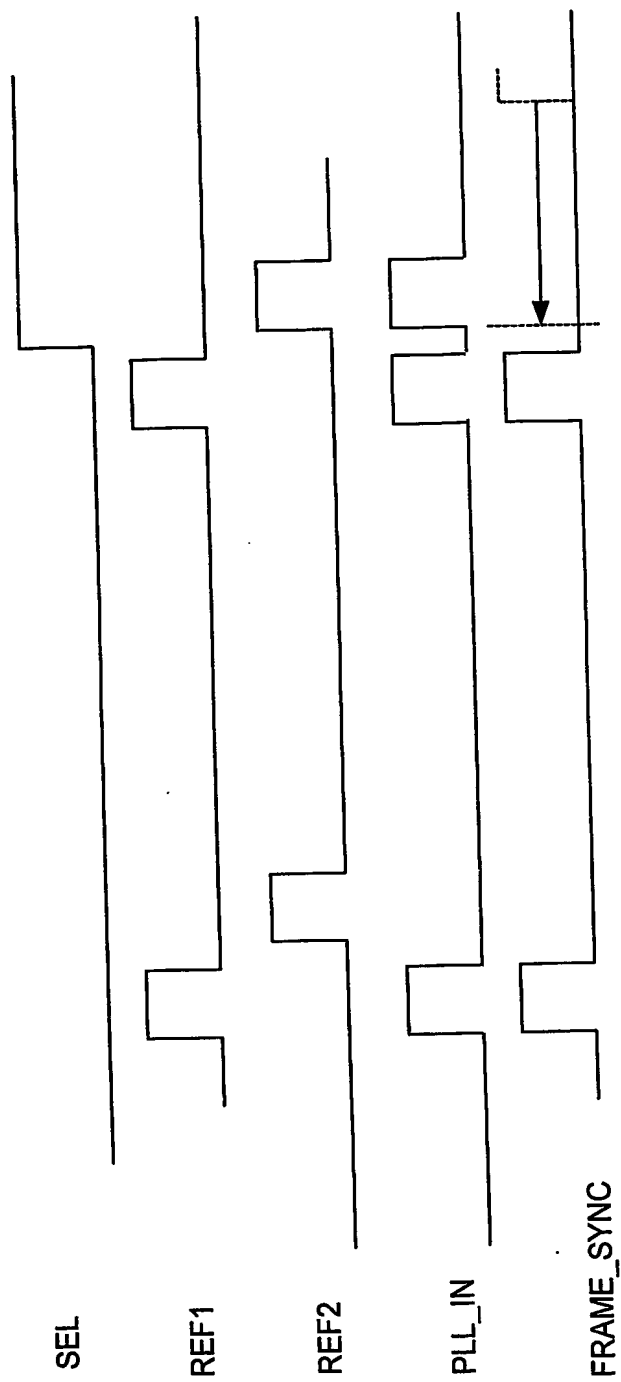


Fig. 2

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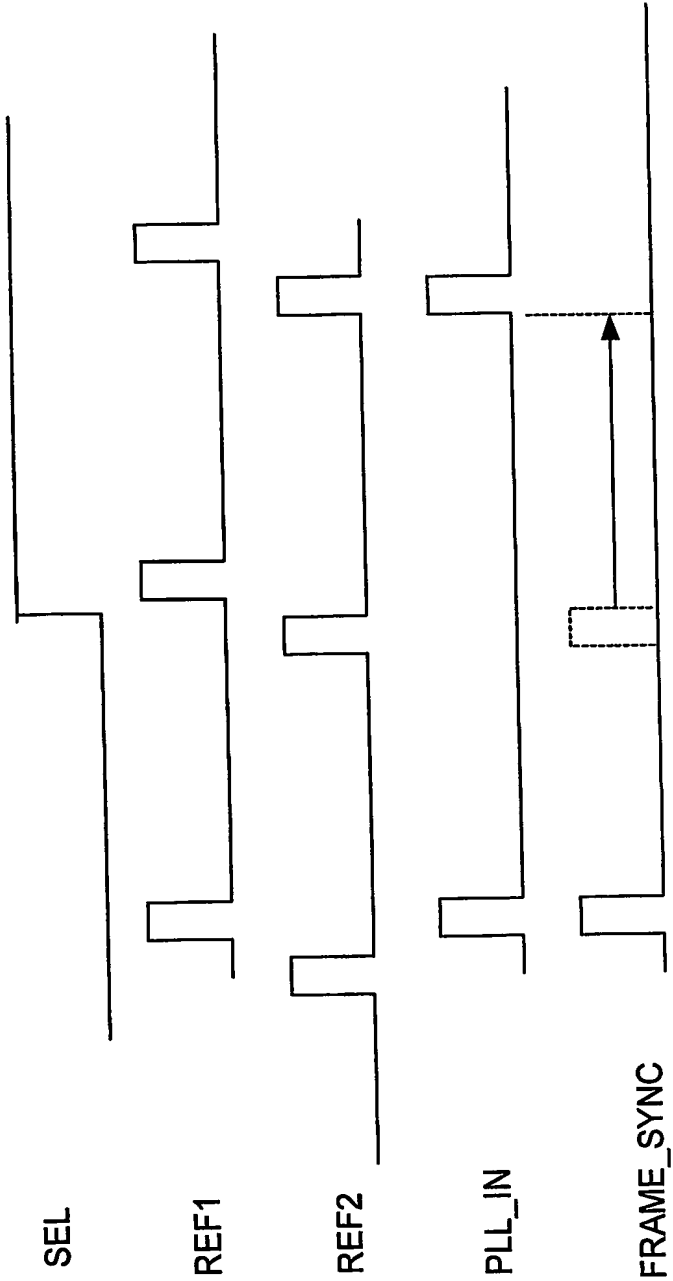


Fig. 3

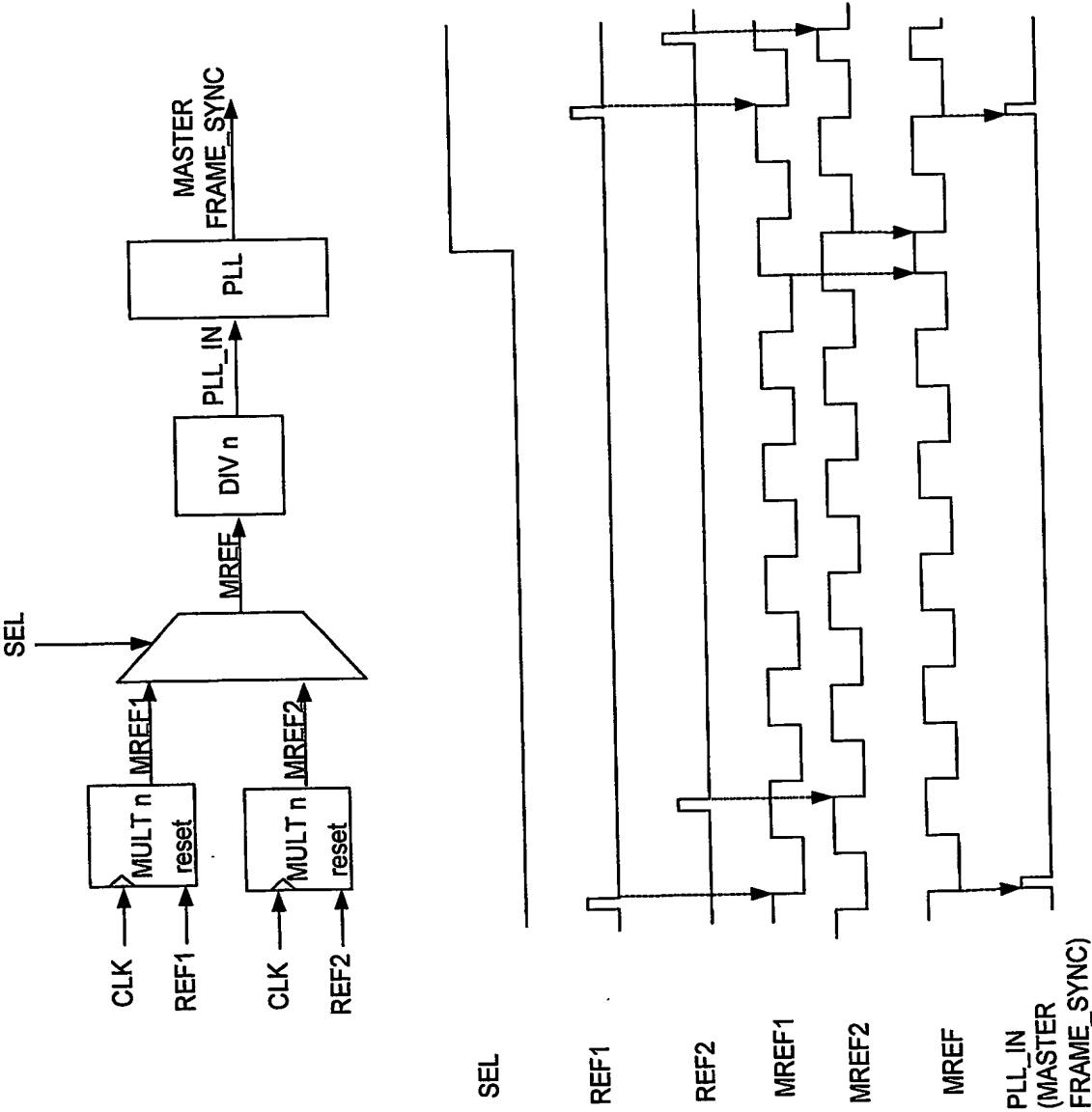


Fig. 4

INTERNATIONAL SEARCH REPORT

International Application No

PCT/NO 02/00304

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H04L7/00 H04Q11/04

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H04J H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EP0-Internal, WPI Data

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WO 98 25367 A (DSC COMMUNICATIONS AS ;NIELSEN ANDERS BOEJE (DK)) 11 June 1998 (1998-06-11) page 2, line 23 -page 3, line 15 abstract; claim 1 ---	1-11
A	DATABASE WPI Section EI, Week 200047 Derwent Publications Ltd., London, GB; Class U23, AN 2000-519766 XP002237855 & JP 2000 201068 A (NEC CORP), 18 July 2000 (2000-07-18) abstract -----	1-10

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

* Special categories of cited documents :

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"&" document member of the same patent family

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Name and mailing address of the ISA

European Patent Office, P.B. 5818 Patentlaan 2
NL - 2280 HV Rijswijk
Tel. (+31-70) 340-2040, Tx. 31 651 epo nl,
Fax: (+31-70) 340-3016

Authorized officer

RALF BOSTRÖM/JA A

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

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Patent document cited in search report		Publication date	Patent family member(s)	Publication date
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